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CLAIMS

1. A method for accessing a memory array, comprising:

reading data and an associated error correction code from a location in the memory array;

storing the data in a FIFO;

modifying at least a portion of the data; and

when writing the modified data to the memory array,

updating the data stored in the FIFO with the modified portion of the data;

calculating a new error correction code based on the updated data in the FIFO; and

storing the updated data and the new error correction code to the location in the memory array.

2. The method of claim 1 wherein modifying at least a portion of the data comprises performing graphics processing operations on the data.

3. The method of claim 1 wherein updating comprises logically combining the stored data and the modified data together.

4. The method of claim 1 wherein updating the data stored in the FIFO with the modified portion of the data comprises:

determining whether a write address corresponds to an address of data previously stored in the FIFO;

accessing the data stored in the FIFO based on the write address if correspondence is determined; and

logically combining the stored data and the modified data together and storing the modified data in the memory location in the FIFO where the data was previously stored.

5. The method of claim 1, further comprising:

substantially concurrent with the reading and storing of data, updating second data previously stored in a second FIFO with a modified portion of the second data; and

substantially concurrent with the updating of the data, reading third data and storing the third data in the second FIFO.

6. The method of claim 1 wherein the memory array is an embedded memory.

7. The method of claim 1, further comprising providing the data read from the location to an output bus for provision to a requesting entity.

8. A method for accessing a memory array, comprising:

reading first data and an associated error correction code from a first location in the memory array;

storing the first data in a first FIFO;

substantially concurrent with the reading and storing of the first data,

updating second data previously stored in a second FIFO with modified data;

calculating a new error correction code based on the updated second data in the second FIFO; and

storing the updated second data and the new error correction code to the location in the memory array from which the original second was read;

modifying at least a portion of the first data;

reading new data from a new location in the memory array;

storing the new data in the second FIFO; and

substantially concurrent with the reading and storing of the new data,

updating the first data stored in a first FIFO with the modified portion of the first data;

calculating a new error correction code based on the updated first data in the first FIFO; and

storing the updated first data and the new error correction code to the first location in the memory array.

9. The method of claim 8 wherein modifying at least a portion of the first data comprises performing graphics processing operations on the first data.

10. The method of claim 8 wherein updating the first and second data comprises logically combining the stored data and the modified data together.

11. The method of claim 8 wherein updating the first and second data stored in the FIFO with the modified portion of the data comprises:

determining whether a write address corresponds to an address of data previously stored in the FIFO;

accessing the data stored in the FIFO based on the write address if correspondence is determined; and

logically combining the stored data and the modified data together and storing the modified data in the memory location in the FIFO where the data was previously stored.

12. The method of claim 8 wherein the memory array is an embedded memory.

13. The method of claim 8, further comprising providing the first data to an output bus for provision to a requesting entity.

14. In a memory system having at least one memory array, a read bus, a write bus, and error correction capability, an apparatus comprising:

a memory having a plurality of memory locations for storing data in a first-in-first-out (FIFO) manner, the memory further having an output from which data is read and an input to which data is written;

a content addressable memory (CAM) coupled to the memory and having an input to receive memory addresses and having a plurality of memory locations for storing memory addresses, each location corresponding to a memory location of the memory, the CAM providing an activation signal to access a memory location of the memory in response to receiving a memory address matching the corresponding stored memory address;

a first switch coupled to the output of the memory to selectively couple the output of the memory to the write bus or an output bus;

a combining circuit having a first input, a second input coupled to the output of the memory, and further having an output coupled to the input of the memory, the combining circuit combining data applied to the first and second inputs and providing the result at the output;

a second switch to selectively couple the first input of the combining circuit to the read bus or an input bus; and

a FIFO control circuit coupled to the combining circuit, the first and second switches, and the memory, in response to receiving a read request, the FIFO control circuit coordinating the storing of the requested data in the memory and providing the requested data to the output bus, and in response to receiving a write request, the FIFO control circuit coordinating the combining of modified data received from the input bus with corresponding original data previously stored in the memory and providing the combined data for error correction code calculation and writing to the location in the memory array from where the corresponding original data was originally read.

15. The apparatus of claim 14 wherein the memory array is an embedded memory array.

16. The apparatus of claim 14 wherein the combining circuit comprises a logic circuit.

17. The apparatus of claim 14 wherein the memory comprises a static random access memory.

18. The apparatus of claim 14, further comprising:

a second memory having a plurality of memory locations for storing data in a first-in-first-out (FIFO) manner, the memory further having an output from which data is read and an input to which data is written;

a second CAM coupled to the second memory and having an input to receive memory addresses and having a plurality of memory locations for storing memory addresses, each location corresponding to a memory location of the second memory, the second CAM providing an activation signal to access a memory location of the second memory in response to receiving a memory address matching the corresponding stored memory address; and

a second combining circuit having a first input, a second input coupled to the output of the second memory, and further having an output coupled to the input of the second memory, the second combining circuit combining data applied to the first and second inputs and providing the result at its output.

19. The apparatus of claim 18 wherein the FIFO control circuit further coordinates the combining of modified data with previously stored data in the second memory substantially concurrently with the storing of the requested data in the memory, and the storing of data in the second memory substantially concurrently with the combining of the modified data with the original data previously stored in the memory.

20. In a memory system having at least one memory array, a read bus, a write bus, and error correction capability, an apparatus comprising:

first and second memories, each memory having a plurality of memory locations for storing data in a first-in-first-out (FIFO) manner and further having an output from which data is read and an input to which data is written;

first and second content addressable memories (CAMs), each CAM coupled to a respective memory and having an input to receive memory addresses and having a plurality of memory locations for storing memory addresses, each location corresponding to a memory location of the respective memory, each CAM providing an activation signal to access a memory location of the respective memory in response to receiving a memory address matching the corresponding stored memory address;

a first selection circuit coupled to the outputs of the memories to selectively couple one of the outputs to the write bus

a second selection circuit coupled to the outputs of the memories to selectively couple one of the outputs to an output bus;

first and second combining circuits, each having a first input, a second input coupled to the output of a respective memory, and further having an output coupled to the input of the respective memory, each combining circuit combining data applied to the first and second inputs and providing the result at the output;

third selection circuit coupled to the read bus and an input bus to selectively coupled the read bus or input bus to the first input of the first combining circuit;

a fourth selection circuit coupled the read bus and an input bus to selectively coupled the read bus or input bus to the first input of the second combining circuit;

a FIFO control circuit coupled to the first and second combining circuits, the first, second, third, and fourth selection circuits, and the first and second memories, in response to receiving a read request, the FIFO control circuit coordinating the storing of the requested data in one of the memories and providing the requested data to the output bus, and in response to receiving a write request, the FIFO control circuit coordinating the combining of modified data

received from the input bus with corresponding original data previously stored in the other memory and providing the combined data for error correction code calculation and writing to the location in the memory array from where the corresponding original data was originally read.

21. The apparatus of claim 20 wherein the first and second memories comprise static random access memories.

22. The apparatus of claim 20 wherein the memory array comprises an embedded memory.

23. The apparatus of claim 20 wherein the first and second combining circuits comprise logic circuits.

24. A graphics processing system, comprising:

at least one memory array;

a read bus coupled to the memory array on which data is retrieved from the memory array;

a write bus coupled to the memory array on which the data is provided to the memory array for storage;

a memory having a plurality of memory locations for storing data in a first-in-first-out (FIFO) manner, the memory further having an output from which data is read and an input to which data is written;

a content addressable memory (CAM) coupled to the memory and having an input to receive memory addresses and having a plurality of memory locations for storing memory addresses, each location corresponding to a memory location of the memory, the CAM providing an activation signal to access a memory location of the memory in response to receiving a memory address matching the corresponding stored memory address;

a first switch coupled to the output of the memory to selectively couple the output of the memory to the write bus or an output bus;

a combining circuit having a first input, a second input coupled to the output of the memory, and further having an output coupled to the input of the memory, the combining circuit combining data applied to the first and second inputs and providing the result at the output;

a second switch to selectively couple the first input of the combining circuit to the read bus or an input bus; and

a FIFO control circuit coupled to the combining circuit, the first and second switches, and the memory, in response to receiving a read request, the FIFO control circuit coordinating the storing of the requested data in the memory and providing the requested data to the output bus, and in response to receiving a write request, the FIFO control circuit coordinating the combining of modified data received from the input bus with corresponding original data previously stored in the memory and providing the combined data for error correction code calculation and writing to the location in the memory array from where the corresponding original data was originally read.

25. The graphics processing system of claim 24, further comprising:

an error correction code (ECC) generator coupled to the write bus and the memory array for generating an ECC in response to writing data to the memory array; and

an ECC check circuit coupled to the memory array and the read bus for confirming the integrity of the data based on an associated ECC.

26. The graphics processing system of claim 24 wherein the memory array is an embedded memory array.

27. The graphics processing system of claim 24 wherein the combining circuit comprises a logic circuit.

28. The graphics processing system of claim 24 wherein the memory comprises a static random access memory.

29. The graphics processing system of claim 24, further comprising:

a second memory having a plurality of memory locations for storing data in a first-in-first-out (FIFO) manner, the memory further having an output from which data is read and an input to which data is written;

a second CAM coupled to the second memory and having an input to receive memory addresses and having a plurality of memory locations for storing memory addresses, each location corresponding to a memory location of the second memory, the second CAM providing an activation signal to access a memory location of the second memory in response to receiving a memory address matching the corresponding stored memory address; and

a second combining circuit having a first input, a second input coupled to the output of the second memory, and further having an output coupled to the input of the second memory, the second combining circuit combining data applied to the first and second inputs and providing the result at its output.

30. The graphics processing system of claim 29 wherein the FIFO control circuit further coordinates the combining of modified data with previously stored data in the second memory substantially concurrently with the storing of the requested data in the memory, and the storing of data in the second memory substantially concurrently with the combining of the modified data with the original data previously stored in the memory.

31. The graphics processing system of claim 24, further comprising a graphics processing pipeline coupled to the output and input busses for processing the data.